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**GARISSA UNIVERSITY**

**UNIVERSITY EXAMINATION 2018/2019 ACADEMIC YEAR FOUR**

**SECOND SEMESTER EXAMINATION**

**SCHOOL OF INFORMATION SCIENCE AND TECHNOLOGY**

**FOR THE DEGREE OF BACHELOR OF INFORMATION SCIENCE**

**COURSE CODE: COM 419**

**COURSE TITLE: COMPUTER SYSTEMS DESIGN**

**EXAMINATION DURATION: 2 HOURS**

**DATE: 06/02/2020 TIME: 09.00-11.00 AM**

**INSTRUCTION TO CANDIDATES**

* **The examination has FIVE (5) questions**
* **Question ONE (1) is COMPULSORY**
* **Choose any other TWO (2) questions from the remaining FOUR (4) questions**
* **Use sketch diagrams to illustrate your answer whenever necessary**
* **Do not carry mobile phones or any other written materials in examination room**
* **Do not write on this paper**

**This paper consists of THREE (3) printed pages *please turn over***

**QUESTION ONE (COMPULSORY)**

1. Describe a von Neuman architecture **[5 marks]**
2. What are the main functional components of a computer system **[8 marks]**
3. List two approaches to dealing with multiple interrupts. **[2 marks]**
4. Consider two possible improvements that can be used to enhance a machine. You can either make multiply instructions run four times faster than before, or make memory access instructions run two times faster than before. You repeatedly run a program that takes 100 seconds to execute. Of this time, 25% is used for multiplication, 40% for memory access instructions, and 35% for other tasks.
5. What will the speedup be if you improve only multiplication? [5%]
6. What will the speedup be if you improve only memory access? [5%]
7. What will the speedup be if both improvements are made? [5%]

**QUESTION TWO**

1. Consider three different processors P1, P2 and P3 executing the same instruction set. P1 has a 3GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4GHz clock rate and a CPI of 2.2.
   1. Which processor has the highest performance expressed in instructions per second? [5%].
   2. If the processors each execute a program in 10 seconds, what is the number of cycles and the number of instructions needed to complete this program? [5%].
2. What is the difference between isolated I/O and memory mapped I/O? **[5 marks]**
3. Explain a typical interrupt process **[5 marks]**

**QUESTION THREE**

1. Explain what is DMA? **[4 marks]**
2. Why does DMA have priority over the CPU when both request a memory transfer  **[4 marks]**
3. Explain vector processing. What is the difference between vector & array processing  **[7 marks]**
4. Explain the organization of virtual memory **[5 marks]**

**QUESTION FOUR**

1. Explain memory hierarchy in a computer system. **[5 marks]**
2. Explain Cache Coherence. **[5 marks]**
3. What is input-output interface? Draw and explain block diagram of input-output interface.

**[5 marks]**

1. Explain Pipelining **[5 marks]**

**QUESTION FIVE**

1. Consider a change to the single-cycle processor that replaces the LOAD instructions with the pair of new instructions in the following way:

Original code: LOAD R1, R2, #100 /\*R1=mem[R2+100] \*/

New code: ADD R4, R2, #100 /\* R4=R2+100 \*/

LOAD R1, R4 /\*R1=mem[R4] \*/

Answer the following questions:

* 1. What is the advantage of such code modification?
  2. What is the disadvantage of such code modification?

1. Assume that the datapath components have the following delays: ALU – 2 nsec, register file read – 1 nsec, instruction memory – 2 nsec, data memory – 2 nsec. You can ignore all other delays and also assume that register file and memory write delays are not accounted for separately. Assume that LOAD instructions account for 30% of all instructions in the program. Would the modification in **a)** above result in a performance improvement or degradation? Explain. **[5 marks]**
2. For the data path component delays as presented in part (c), determine the maximum percentage of LOAD instructions in a program, so that the proposed modification still has a positive impact on performance. Explain. **[5 marks]**